


```
graph TD
    CPU[PROCESSOR 202] --- BUS
    subgraph MEMORY_204 [MEMORY 204]
        EDITOR_206[EDITOR 206]
        subgraph EDITOR_206_BOX [ ]
            ERC[EVENT ROUTING CONTROLLER 208]
        end
        subgraph SERVICES [ ]
            D1[DESIGNER EXT. MECH. 210]
            S[SELECTION SERVICES COMPONENT 212]
            H[HIGHLIGHT RENDERING SERVICES 214]
        end
        D1 --- BUS
        S --- BUS
        H --- BUS
    end
    EDITOR_206 --- SERVICES
    subgraph DESIGNERS [ ]
        D2[DESIGNER 216]
        D3[DESIGNER 218]
        D4[DESIGNER 220]
    end
    D1 --- D2
    D1 --- D3
    D1 --- D4
```

The diagram illustrates a computer system architecture. At the top, a box labeled "COMPUTER 200" contains a "PROCESSOR 202" on the left and a large "MEMORY 204" block on the right. Inside the "MEMORY 204" block, there is an "EDITOR 206" at the top. Below the editor is a box containing an "EVENT ROUTING CONTROLLER 208". Further down, there are three boxes: "DESIGNER EXT. MECH. 210", "SELECTION SERVICES COMPONENT 212", and "HIGHLIGHT RENDERING SERVICES 214". These three boxes are connected to a horizontal bus line. Below this bus line are three more boxes, each labeled "DESIGNER 216", "DESIGNER 218", and "DESIGNER 220". The "DESIGNER EXT. MECH. 210" box is connected to all three "DESIGNER" boxes (216, 218, and 220). The "SELECTION SERVICES COMPONENT 212" and "HIGHLIGHT RENDERING SERVICES 214" boxes are also connected to the same bus line, which in turn connects to the three "DESIGNER" boxes.

Fig. 2

DESIGNER
REGISTRY
303

EVENT OBJ. I/F
316

Fig. 3

[illegible]

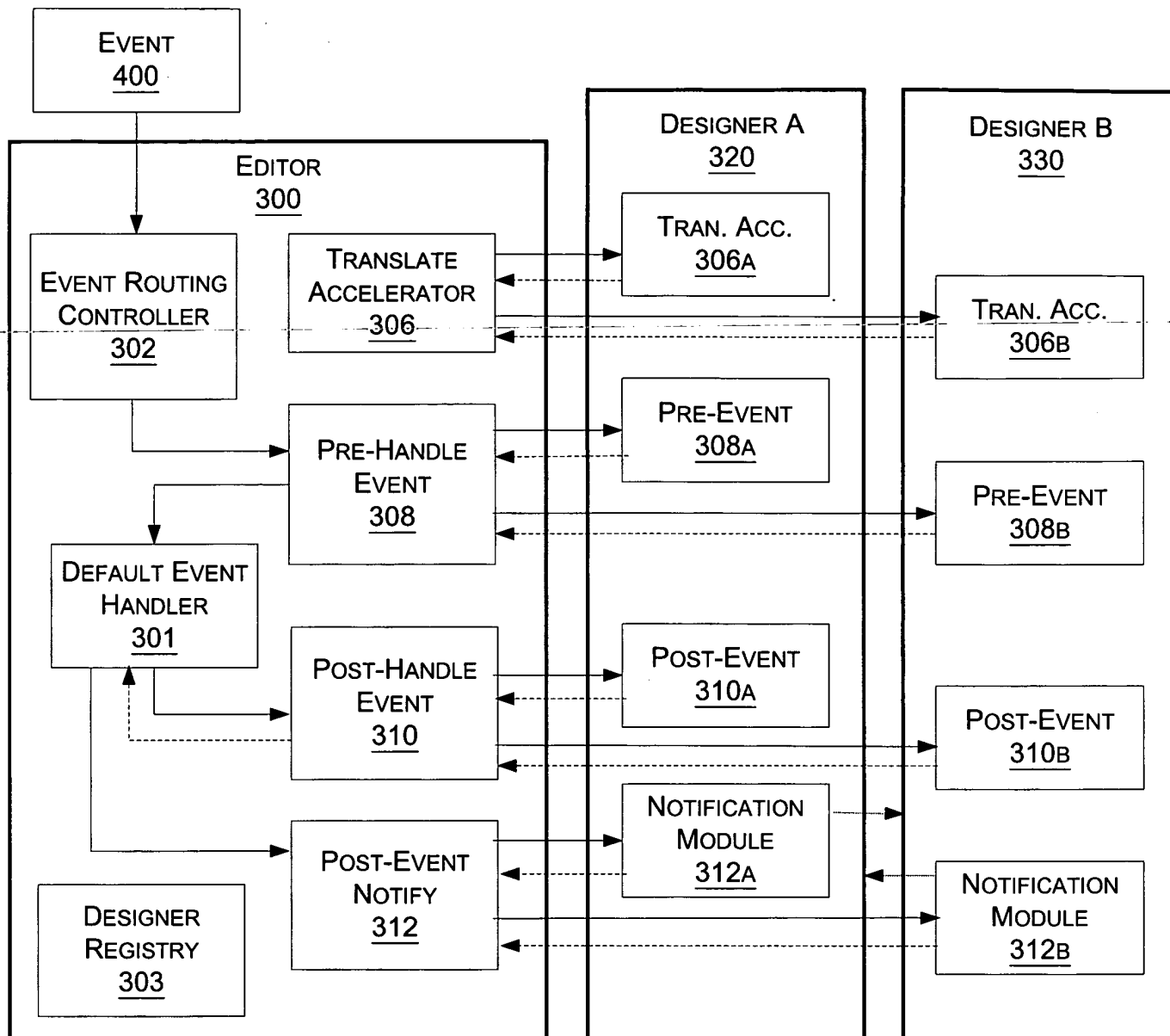


Fig. 4

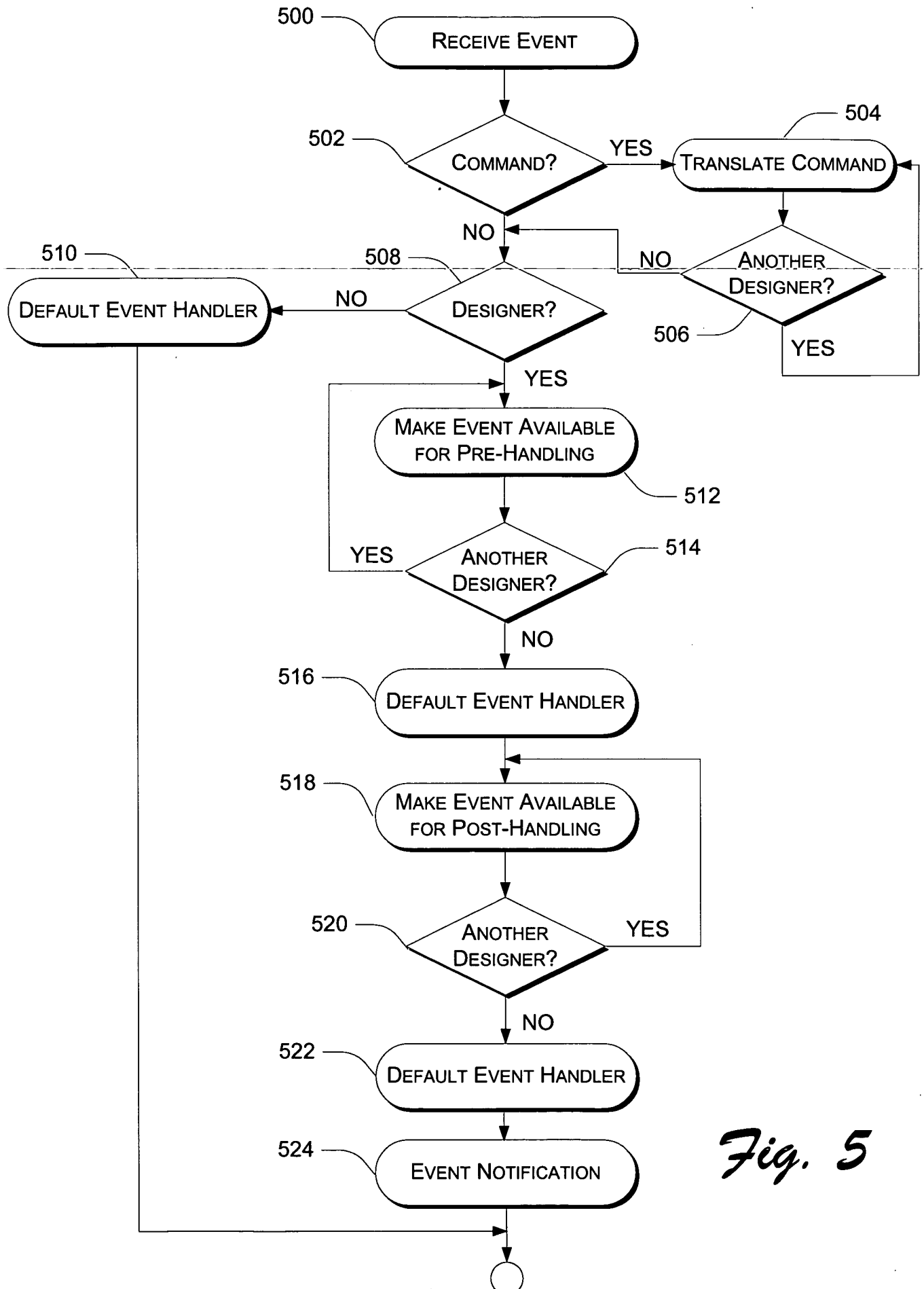


Fig. 5

DESIGNER INTERFACE
702

HIGHLIGHT SERVICES COMPONENT

ADD SEGMENT
712

REMOVE SEGMENT
716

HIGHLIGHT SEGMENT INTERFACE

Fig. 7